CLAIMS

What is claimed is:

1. A method of manufacturing a flash memory Electrically-Erasable Programmable Read-Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of source dopants is decreased and having low V_{SS} resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, a drain, a floating gate, a control gate and a substrate, the method comprising:

(a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;

(b) forming a first source mask exposing the source regions and portions of the gates;

(c) implanting the exposed source regions with n dopant ions;

(d) removing the first source mask;

(e) forming a second source mask exposing a portion of the source regions;

(f) implanting the exposed portions of the source regions with n^+ dopant ions; and

(g) removing the second source mask.

2. The method of Claim 1 further comprising annealing the device.

3. The method of Claim 1 wherein step (c) is accomplished by implanting n dopant ions at a low dosage and at low energy.

4. The method of Claim 1 wherein step (f) is accomplished by implanting n dopant ions a high dosage and at high energy.

5. A method of manufacturing a flash memory Electrically-Erasable Programmable Read-Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of source dopants is decreased and having low V_{SS} resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, a drain, a floating gate, a control gate and a substrate, the method comprising:

(a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;

(b) forming a source mask exposing portions of the source regions;

(c) implanting the exposed portions of the source regions with n+ dopant ions; and

(d) removing the source mask.

6. The method of Claim 5 further comprising annealing the device.

7. The method of Claim 5 wherein step (c) is accomplished by implanting n dopant ions at a high dosage and at high energy.